DISPLAY APPARATUS AND DISPLAY DRIVING METHOD FOR EFFECTIVELY ELIMINATING THE OCCURRENCE OF A MOVING IMAGE FALSE CONTOUR

CROSS REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2003-187702, filed on June 30, 2003, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a display apparatus and a display driving method, and more particularly to a display apparatus and a display driving method suitable for driving a plasma display panel (PDP).

2. Description of the Related Art

With the recent trend toward larger-screen displays, the need for thin display apparatuses has been increasing, and various types of thin display apparatus have been commercially implemented. Examples include matrix panels that display images by directly using digital signals, such as PDPs and other gas discharge display panels, digital micromirror devices (DMDs), EL display devices, fluorescent display tubes, and liquid crystal display devices. Among such thin display devices, gas discharge display panels are considered to be the most promising candidate for large-area, direct-view HDTV (high-definition television) display devices, because of the simple production process which facilitates fabrication of larger-area displays, a self-luminescent property which ensures good display quality, and a high response speed.

A plasma display apparatus that utilizes a surface discharge has a structure such that a pair of electrodes are formed on the inner surface of a front

glass substrate and a rare gas is filled therein. When a voltage is applied between the electrodes, a surface discharge occurs at the surface of a protective layer and a dielectric layer formed on the electrode surface, resulting in the emission of ultraviolet light. The inner surface of a rear glass substrate is coated with phosphors of three primary colors, red (R), green (G), and blue (B), which when excited by the ultraviolet light, produce visible light to achieve a color display.

In the plasma display apparatus, each field (frame) is divided into a plurality of weighted subfields (SFs: light emission blocks) each comprising a plurality of sustain discharge pulses (sustain pulses), and a gray scale display is achieved by combining these subfields. In a display apparatus that achieves a gray scale display by combining a plurality of such weighted subfields, a phenomenon can occur in which an unnatural color contour, which normally should not exist, appears on the surface of a moving image due to the persistence of human vision, etc. This phenomenon is generally known as "moving image false contour (or moving image pseudo contour." In particular, when a person in a displayed image moves, a green or red color band occurs, for example, on the contour of the person's face or other flesh-colored portions, and this greatly degrades the picture quality.

In the prior art, techniques for improving the picture quality by reducing the moving image false contour phenomenon are proposed in Japanese Patent No. 3322809 (Japanese Unexamined Patent Publication (Kokai) No. 10-31455: JPP'455) and Japanese Unexamined Patent Publication (Kokai) No. 11-85101 (JPP'101). In the prior art, there is also proposed, in Japanese Patent No. 3357666 (Japanese Unexamined Patent Publication (Kokai) No. 2002-82649: JPP'649), a display apparatus and a display driving method in which, by using an error diffusion technique, the maximum gray scale level and the number of reproducible gray scale levels are made

sufficiently large without increasing the number of subfields, while at the same time achieving enhancement in the reproducibility of low gray scale levels.

The prior art and its associated problems will be described later with reference to the accompanying drawings.

SUMMARY OF THE INVENTION

According to the present invention, there is provided a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method, comprising a gain control circuit compressing the number of gray scale levels of an input signal and outputting a first intermediate image signal with a first number of gray scale levels; a sub gain control circuit receiving the first intermediate image signal, compressing the number of gray scale levels of the first intermediate image signal, and outputting a second intermediate image signal with a second number of gray scale levels; and an error diffusion circuit receiving the second intermediate image signal and increasing the number of gray scale levels by simulating additional gray scale levels through error diffusion.

The display apparatus may further comprise a first subfield arrangement setting unit forming one field with a plurality of subfields so that the number of gray scale levels becomes equal to the first number of gray scale levels; and a second subfield arrangement setting unit forming one field with a plurality of subfields so that the number of gray scale levels becomes equal to the second number of gray scale levels which is smaller than the first number of gray scale levels. The image signal may be any one of RGB signals of red, green, and blue; and the gain control circuit, the sub gain control circuit, and the error diffusion circuit may be provided for each of the RGB signals.

According to the present invention, there is also

provided a display apparatus which expresses luminance by varying light emission time length and displays gray scale by using a subfield method, comprising a main path generating, from an input signal with a first number of gray scale levels, a first image signal with a second number of gray scale levels which is smaller than the first number of gray scale levels; a sub path generating a second image signal with a third number of gray scale levels which is smaller than the second number of gray scale levels; a switch circuit outputting the first image signal generated by the main path or the second image signal generated by the sub path by switching therebetween; and a path switching control section detecting, from the input image signal and a signal obtained by processing the input image signal, a motion region where the amount of image motion is larger than a predetermined value, and in the motion region, switching the switch circuit from the first image signal to the second image signal, and wherein the main path comprises a gain control circuit receiving the input image signal with the first number of gray scale levels and outputting a first intermediate image signal with a fourth number of gray scale levels; a sub gain control circuit receiving the first intermediate image signal and outputting a second intermediate image signal which has the second number of gray scale levels; and an error diffusion circuit receiving an output signal of the sub gain control circuit, applying error diffusion, and outputting the first image signal.

The display apparatus may further comprise a first subfield arrangement setting unit forming one field with a plurality of subfields so that the number of gray scale levels becomes equal to the fourth number of gray scale levels; and a second subfield arrangement setting unit forming one field with a plurality of subfields so that the number of gray scale levels becomes equal to the second number of gray scale levels which is smaller than

the fourth number of gray scale levels. The first subfield arrangement setting unit may assign a weight 1 to a first subfield and a weight 3 or larger to a second subfield.

The ratio of the weight assigned to each subfield in the first subfield arrangement setting unit to the weight assigned to each subfield in the second subfield arrangement setting unit may be approximately m:n (where m and n are natural numbers, and $n < m$). The subfields to be set for light emission when displaying an arbitrary gray scale level may except low gray scale levels, the second subfield arrangement setting unit may set the most heavily weighted subfield for light emission along with at least one of the other subfields.

The first subfield arrangement setting unit may set the arrangement of the plurality of subfields to achieve the fourth number of gray scale levels, m, and the second subfield arrangement setting unit may set the arrangement of the plurality of subfields to achieve the second number of gray scale levels, n (where m and n are natural numbers, and $n < m$). The number of gray scale levels, m, generated by the first subfield arrangement setting unit and the number of gray scale levels, n, generated by the second subfield arrangement setting unit may have a relationship such that $(m-1):(n-1)$ is substantially equal to a ratio of integers. The ratio $(m-1):(n-1)$ may be 2:3, 4:5, or 4:7.

The sub gain control circuit may generate the second intermediate image signal with the second number of gray scale levels by compressing the first intermediate image signal with the fourth number of gray scale levels through multiplication with $(n-1)/(m-1)$. The sub gain control circuit may divide n gray scale levels into a plurality of regions, and may perform the multiplication with the coefficient $(n-1)/(m-1)$ by approximating the divided regions by a broken line formed of a set of straight line segments each having a slope equal to a

submultiple of a natural number. The slope of each of the straight line segments in the broken line approximation may be selected from the group consisting of 1, 1/2, 1/3, and 1/4.

The display apparatus may further comprise a weight setting unit multiplying each weight by (m-1)/(n-1) in order to expand the first image signal compressed through the multiplication with the coefficient (n-1)/(m-1) in the sub gain control circuit and output via the error diffusion circuit. The image signal may be any one of RGB signals of red, green, and blue; and the main path, the sub path, the switch circuit, the path switching control section, the gain control circuit, the sub gain control circuit, and the error diffusion circuit may be provided for each of the RGB signals. The display apparatus may be a plasma display apparatus.

Further, according to the present invention, there is provided a display driving method for driving a display that expresses luminance by varying light emission time length and displays gray scale by using a subfield method, the driving method comprising the steps of generating a first intermediate image signal with a first number of gray scale levels by compressing the number of gray scale levels of an input signal; generating a second intermediate image signal with a second number of gray scale levels by further compressing the number of gray scale levels of the first intermediate image signal; and generating an output image signal by applying error diffusion to the second intermediate image signal.

The display driving method may further comprise the steps of performing first subfield arrangement setting to form one field with a plurality of subfields so that the number of gray scale levels becomes equal to the first number of gray scale levels; and performing second subfield arrangement setting to form one field with a plurality of subfields so that the number of gray scale

levels becomes equal to the second number of gray scale levels which is smaller than the first number of gray scale levels. The image signal may be any one of RGB signals of red, green, and blue; and gain control circuit, the sub gain control circuit, and the error diffusion circuit may be provided for each of the RGB signals.

In addition, according to the present invention, there is also provided a display driving method for driving a display that expresses luminance by varying light emission time length and displays gray scale by using a subfield method, the display comprising a main path generating, from an input signal with a first number of gray scale levels, a first image signal with a second number of gray scale levels which is smaller than the first number of gray scale levels; a sub path generating a second image signal with a third number of gray scale levels which is smaller than the second number of gray scale levels; a switch circuit outputting the first image signal generated by the main path or the second image signal generated by the sub path by switching therebetween; and a path switching control section detecting, from the input image signal and a signal obtained by processing the input image signal, a motion region where the amount of image motion is larger than a predetermined value, and in the motion region, switching the switch circuit from the first image signal to the second image signal, and wherein, in the main path a first computation is performed to compress the input image signal with the first number of gray scale levels, thereby generating a first intermediate image signal with a fourth number of gray scale levels; a second computation is performed to further compress the first intermediate image signal, thereby outputting a second intermediate image signal having the second number of gray scale levels which is smaller than the fourth number of gray scale levels; and error diffusion is applied to

the sub gain control circuit, thereby generating the first image signal.

The display driving method may further comprise the steps of performing first subfield arrangement setting to form one field with a plurality of subfields so that the number of gray scale levels becomes equal to the fourth number of gray scale levels; and performing second subfield arrangement setting to form one field with a plurality of subfields so that the number of gray scale levels becomes equal to the second number of gray scale levels which is smaller than the fourth number of gray scale levels.

In the first subfield arrangement setting, a weight 1 may be assigned to a first subfield and a weight 3 or larger is assigned to a second subfield. The ratio of the weight assigned to each subfield in the first subfield arrangement setting to the weight assigned to each subfield in the second subfield arrangement setting may be approximately m:n (where m and n are natural numbers, and $n < m$). In the second subfield arrangement setting, of the subfields to be set for light emission when displaying an arbitrary gray scale level except low gray scale levels, the most heavily weighted subfield may be set for light emission along with at least one of the other subfields.

The first subfield arrangement setting may set the arrangement of the plurality of subfields to achieve the fourth number of gray scale levels, m, and the second subfield arrangement setting may set the arrangement of the plurality of subfields to achieve the second number of gray scale levels, n (where m and n are natural numbers, and $n < m$). The number of gray scale levels, m, generated in the first subfield arrangement setting and the number of gray scale levels, n, generated in the second subfield arrangement setting may have a relationship such that $(m-1):(n-1)$ is substantially equal to a ratio of integers. The ratio $(m-1):(n-1)$ may be

2:3, 4:5, or 4:7.

The generation of the second intermediate image signal performed by further compressing the number of gray scale levels of the first intermediate image signal may be accomplished by multiplying the first intermediate image signal by (n-1)/(m-1). The generation of the second intermediate image signal performed by further compressing the number of gray scale levels of the first intermediate image signal may comprise dividing n gray scale levels into a plurality of regions and multiplying the first intermediate image signal by (n-1)/(m-1) by approximating the divided regions by a broken line formed of a set of straight line segments each having a slope equal to a submultiple of a natural number. The slope of each of the straight line segments in the broken line approximation may be selected from the group consisting of 1, 1/2, 1/3, and 1/4.

The display driving method may further comprise the step of multiplying each weight by (m-1)/(n-1) in order to expand the output image signal compressed through the multiplication with the coefficient (n-1)/(m-1) and output after the error diffusion. The image signal may be any one of RGB signals of red, green, and blue; and the main path, the sub path, the switch circuit, the path switching control section, the gain control circuit, the sub gain control circuit, and the error diffusion circuit may be provided for each of the RGB signals. The display apparatus may be a plasma display apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description of the preferred embodiments as set forth below with reference to the accompanying drawings, wherein:

Fig. 1 is a block diagram schematically showing one example of a plasma display apparatus;

Fig. 2 is a diagram showing one example of a gray scale driving sequence in a prior art plasma display

apparatus;

Fig. 3 is a block diagram showing one example of an image processing circuit in the prior art plasma display apparatus;

Fig. 4 is a diagram showing another example of the gray scale driving sequence in the plasma display apparatus;

Fig. 5 is a diagram showing one example of an arrangement of light emission subfield periods for each luminance level in a main path;

Fig. 6 is a diagram showing one example of an arrangement of light emission subfield periods for each luminance level in a sub path;

Fig. 7 is a block diagram showing one example of an image feature judging section in the image processing circuit of Fig. 3;

Fig. 8 is a block diagram showing one example of an image processing circuit in a plasma display apparatus according to the present invention;

Fig. 9 is a diagram (part 1) showing one example of a subfield light emission table which is applied to the plasma display apparatus according to the present invention;

Fig. 10 is a diagram (part 2) showing the example of the subfield light emission table applied to the plasma display apparatus according to the present invention;

Fig. 11 is a diagram (part 3) showing the example of the subfield light emission table applied to the plasma display apparatus according to the present invention;

Fig. 12 is a diagram (part 4) showing the example of the subfield light emission table applied to the plasma display apparatus according to the present invention;

Fig. 13 is a diagram showing one example of a subfield light emission table for the sub path, which is applied to the plasma display apparatus according to the present invention;

Fig. 14 is a diagram (part 1) showing another

example of the subfield light emission table applied to the plasma display apparatus according to the present invention;

Fig. 15 is a diagram (part 2) showing the example of the subfield light emission table applied to the plasma display apparatus according to the present invention;

Fig. 16 is a diagram (part 3) showing the example of the subfield light emission table applied to the plasma display apparatus according to the present invention;

Fig. 17 is a diagram (part 4) showing the example of the subfield light emission table applied to the plasma display apparatus according to the present invention;

Fig. 18 is a diagram showing another example of the subfield light emission table for the sub path, which is applied to the plasma display apparatus according to the present invention;

Fig. 19 is a block diagram schematically showing a sub gain control circuit in a first embodiment of the plasma display apparatus according to the present invention;

Fig. 20 is a diagram for explaining the sub gain control circuit shown in Fig. 19;

Fig. 21 is a diagram (part 1) for explaining the operation of the sub gain control circuit shown in Fig. 19;

Fig. 22 is a diagram (part 2) for explaining the operation of the sub gain control circuit shown in Fig. 19;

Fig. 23 is a diagram (part 3) for explaining the operation of the sub gain control circuit shown in Fig. 19;

Fig. 24 is a diagram (part 4) for explaining the operation of the sub gain control circuit shown in Fig. 19;

Fig. 25 is a diagram (part 5) for explaining the operation of the sub gain control circuit shown in Fig. 19;

Fig. 26 is a diagram (part 6) for explaining the operation of the sub gain control circuit shown in Fig. 19;

Fig. 27 is a block diagram schematically showing a sub gain control circuit in a second embodiment of the plasma display apparatus according to the present invention;

Fig. 28 is a diagram for explaining the sub gain control circuit shown in Fig. 27;

Fig. 29 is a diagram (part 1) for explaining the operation of the sub gain control circuit shown in Fig. 27;

Fig. 30 is a diagram (part 2) for explaining the operation of the sub gain control circuit shown in Fig. 27;

Fig. 31 is a diagram (part 3) for explaining the operation of the sub gain control circuit shown in Fig. 27;

Fig. 32 is a diagram (part 4) for explaining the operation of the sub gain control circuit shown in Fig. 27;

Fig. 33 is a diagram (part 5) for explaining the operation of the sub gain control circuit shown in Fig. 27;

Fig. 34 is a block diagram schematically showing a sub gain control circuit in a third embodiment of the plasma display apparatus according to the present invention;

Fig. 35 is a diagram for explaining the sub gain control circuit shown in Fig. 34;

Fig. 36 is a diagram (part 1) for explaining the operation of the sub gain control circuit shown in Fig. 34;

Fig. 37 is a diagram (part 2) for explaining the operation of the sub gain control circuit shown in Fig. 34;

Fig. 38 is a diagram (part 3) for explaining the

operation of the sub gain control circuit shown in Fig. 34;

Fig. 39 is a diagram (part 4) for explaining the operation of the sub gain control circuit shown in Fig. 34;

Fig. 40 is a diagram (part 5) for explaining the operation of the sub gain control circuit shown in Fig. 34;

Fig. 41 is a diagram (part 6) for explaining the operation of the sub gain control circuit shown in Fig. 34;

Fig. 42 is a diagram (part 7) for explaining the operation of the sub gain control circuit shown in Fig. 34;

Fig. 43 is a block diagram schematically showing a sub gain control circuit in a fourth embodiment of the plasma display apparatus according to the present invention;

Fig. 44 is a diagram for explaining the sub gain control circuit shown in Fig. 43;

Fig. 45 is a diagram (part 1) for explaining the operation of the sub gain control circuit shown in Fig. 43;

Fig. 46 is a diagram (part 2) for explaining the operation of the sub gain control circuit shown in Fig. 43;

Fig. 47 is a diagram (part 3) for explaining the operation of the sub gain control circuit shown in Fig. 43;

Fig. 48 is a diagram (part 4) for explaining the operation of the sub gain control circuit shown in Fig. 43;

Fig. 49 is a diagram (part 5) for explaining the operation of the sub gain control circuit shown in Fig. 43;

Figs. 50A and 50B are block diagrams of essential portions, showing a comparison between the configuration

in which the sub gain control circuit is used and the configuration in which the sub gain control circuit is not used in the plasma display apparatus;

Fig. 51 is a diagram (part 1) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention;

Fig. 52 is a diagram (part 2) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention;

Fig. 53 is a diagram (part 3) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention;

Fig. 54 is a diagram (part 4) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention;

Fig. 55 is a diagram (part 5) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention;

Fig. 56 is a diagram (part 6) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention;

Fig. 57 is a diagram (part 7) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention;

Fig. 58 is a diagram (part 8) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention;

Fig. 59 is a diagram (part 9) for explaining the effect of using the sub gain control circuit in the

plasma display apparatus according to the present invention; and

Fig. 60 is a diagram (part 10) for explaining the effect of using the sub gain control circuit in the plasma display apparatus according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before proceeding to the detailed description of the preferred embodiments of the present invention, the prior art display apparatuses and display driving methods and their associated problems will be described with reference to the drawings.

Figure 1 is a block diagram schematically showing one example of a plasma display apparatus. In Fig. 1, reference numeral 1 is an image processing circuit, 2 is an light emission time control circuit, 3 is a PDP driving circuit, and 4 is a PDP. For convenience of illustration, in Fig. 1 the PDP 4 is shown inside the PDP driving circuit 3.

As shown in Fig. 1, the plasma display apparatus comprises: the image processing circuit 1 which processes image signals of R, G, and B colors; the light emission time control circuit 2 which controls the light emission time for light emission in the PDP 4 in accordance with output signals of the image processing circuit 1; and the PDP driving circuit 3 which drives the PDP 4 in accordance with the output of the light emission time control circuit 2. The PDP driving circuit 3 comprises a field memory 31, a memory controller 32, an SF weight table 33, a number-of-SUSs setting circuit 34, a controller 35, a scan driver 36, a sustain driver 37, and an address driver 38. Here, the SF weight table 33 is a memory device which stores the ratio of the number of SUSs (weight) for each subfield, and the number-of-SUSs setting circuit 34 is a circuit which, in accordance with the SF weight table 33, sets the number of SUSs with which each SF is caused to emit light.

The light emission time control circuit 2 receives the output signals of the image processing circuit 1, converts them into data indicating the times and the subfields for light emission to achieve desired gray scale levels, and supplies the converted data to the PDP driving circuit 3. The converted data supplied from the light emission time control circuit 2 is written to and read from the field memory 31 under the control of the memory controller 32. Here, the light emission time control circuit 2 and the field memory 31 together constitute a subfield converting section.

The address driver 38 drives the PDP 4 based on the data read from the field memory 31. The controller 35 receives the output of the SF weight table 33 via the number-of-SUSs setting circuit 34, and controls the driving of the PDP 4 by controlling the scan driver 36 as well as the sustain driver 37. When the PDP 4 is driven by the scan driver 36 and the address driver 38, a wall charge is formed on each pixel to be activated for light emission in each subfield, and when the PDP 4 is driven by the sustain driver 37, sustain discharge occurs.

Figure 2 is a diagram showing one example of a gray scale driving sequence in the prior art plasma display apparatus.

As shown in Fig. 2, in the gray scale driving sequence for the plasma display apparatus, each field for forming one complete image is divided, for example, into a plurality of subfields (for example, SF1 to SF6), and a gray scale display of the image is achieved by controlling the sustain period (light emission period) in each subfield. Each subfield comprises an address period in which a wall charge is formed for all the pixels that are to be activated for light emission in the subfield period, and the sustain period which determines the luminance level. Accordingly, if the number of subfields is increased, the number of address periods increases correspondingly, and the sustain periods for light

emission are relatively shortened, resulting in reduced screen brightness.

In a PDP, in order to increase the number of reproducible gray scale levels by using the limited number of subfields, a gray scale driving method is commonly employed that drives the PDP by using the sustain periods proportional to the bit weights as shown in Fig. 2. That is, in the example shown in Fig. 2, one field is made up of six subfield periods SF1 to SF6, and 64 levels of gray scale are reproduced by a 6-bit image signal (image data) corresponding to each subfield. The sustain periods in the respective subfield periods SF1 to SF6 are indicated by hatching by assuming, for convenience, that light emission is produced in each subfield period, and the time (length) ratio is set as SF1:SF2:SF3:SF4:SF5:SF6 = 1:2:4:8:16:32. Here, one field period is about 16.7 ms.

When displaying a moving image on the PDP using the above gray scale driving sequence, a phenomenon can occur in which an unnatural color contour, which normally should not exist, appears on the surface of the moving image due to the persistence of human vision, etc. The contour occurring in this phenomenon is generally known as "moving image false contour". This moving image false contour becomes particularly noticeable when a person on the display screen moves; for example, a green or red color band occurs on the contour of the person's face or other flesh-colored portions, degrading the picture quality.

In the prior art, techniques for improving the picture quality by reducing the moving image false contour phenomenon are proposed in JPP'455 and JPP'101.

Figure 3 is a block diagram showing one example of an image processing circuit in the prior art plasma display apparatus, which is applied, for example, as the image processing circuit 1 in the plasma display apparatus shown in Fig. 1.

As shown in Fig. 3, the image processing circuit 1 roughly comprises a main path 11, a sub path 12, a switch circuit 13, and an image feature judging section 14. Each input image signal is supplied in parallel to the main path 11, the sub path 12, and to a part of the image feature judging section 14. The output of the main path 11 is supplied to the switch circuit 13, as well as to a part of the image feature judging section 14. The output of the sub path 12 is supplied to the switch circuit 13. Based on a path select/switch signal supplied from the image feature judging section 14, the switch circuit 13 supplies the image signal from the main path 11 or the sub path 12, whichever is selected, to the light emission time control circuit 2 shown in Fig. 1.

The main path 11 includes a gain control circuit 111 which is supplied with the input image signal, and an error diffusion circuit 112 which is supplied with an output signal of the gain control circuit 111. On the other hand, the sub path 12 includes a distortion correction circuit 121 which is supplied with the input image signal, a gain control circuit 122 which is supplied with an output signal of the distortion correction circuit 121, an error diffusion circuit 123 which is supplied with an output signal of the gain control circuit 122, and a data matching circuit 124 which is supplied with an output signal of the error diffusion circuit 123.

The image feature judging section 14 includes an RGB matrix circuit 141 which is supplied with the input image signals, an edge detection circuit 142 and a motion region detection circuit 143 each of which is supplied with an output signal of the RGB matrix circuit 141, a first judging circuit 144 which is supplied with output signals of the edge detection circuit 142 and the motion region detection circuit 143, a level detection circuit 145 which is supplied with the output signal of the main path, and a second judging circuit 146 which is supplied

with output signals of the first judging circuit 144 and the level detection circuit 145. Here, when each field comprises eight subfields, and the ratio of the number of sustain pulses among the respective subfield periods is set as SF1:SF2:SF3:SF4:SF5:SF6:SF7:SF8 = 12:8:4:2:1:4:8:12, for example, the main path 11 represents 52 real gray scale levels with a 6-bit output for each of the RGB signals; in this case, the number of reproducible gray scale levels for each color is 52 from level 0 to level 51.

In the image processing circuit shown in Fig. 3, rather than performing image motion detection and edge detection for each of the three RGB colors independently of each other, the RGB matrix circuit 141 generates a luminance signal from the RGB signals and, based on the generated luminance signal, the edge detection circuit 142 detects an edge of the image and the motion region detection circuit 143 detects a motion region in the image, thereby achieving a reduction in the amount of circuitry. The luminance signal Y can be generated using a generating equation such as $Y = 0.30R + 0.59G + 0.11B$.

The highest luminance level that can be displayed on the PDP 4 via the main path 11 is 51 with a 6-bit output, while the highest luminance level of the input image signal is 255 with an 8-bit input. Accordingly, the gain control circuit 111 multiplies the input image signal with a gain coefficient $51 \times 2^{8-6}/255 = 204/255$. As a result of the multiplication with this gain coefficient, the error diffusion circuit 112 at the next stage can apply error diffusion over the entire range of the input image signal. The gain control circuit 111 can be constructed from a conventional multiplier or from a memory such as a RAM (Random Access Memory) or a ROM (Read Only Memory).

By applying error diffusion to the image signal obtained via the gain control circuit 111, the error diffusion circuit 112 simulates intermediate gray levels

to increase the number of gray scale levels. Since the number of reproducible gray scale levels in the main path 11 is 52, the output bit count of the error diffusion circuit 112 is 6.

The sub path 12 represents 9 real gray scale levels with a 4-bit output; in this case, the number of reproducible gray scale levels for each of the RGB colors is 9 from level 0 to level 8.

The sub path 12 can represent gray scale in 9 steps from 0 to 8, but the amount of luminance does not increase equally, but increases unequally such as 0, 1, 3, 7, 11, and so on. As a result, a correction that is an inverse function of the display characteristic after the error diffusion must be applied to obtain a linear display characteristic as a whole. In the distortion correction circuit 121, such an inverse function characteristic is stored in a ROM or RAM table.

Figure 4 is a diagram showing another example of the gray scale driving sequence in the plasma display apparatus, Fig. 5 is a diagram showing one example of an arrangement of light emission subfield periods for each luminance level in the main path, and Fig. 6 is a diagram showing one example of an arrangement of light emission subfield periods for each luminance level in the sub path.

When each field is made up of eight subfields SF1 to SF8, and the ratio of the number of sustain pulses (the luminance level ratio) is set as SF1:SF2:SF3:SF4:SF5:SF6:SF7:SF8 = 12:8:4:2:1:4:8:12, as described above, the gray scale driving sequence is as shown in Fig. 4.

In this case, the main path 11 can reproduce the input image signal in 52 real gray scale levels, and the arrangement of the light emission subfield periods for each luminance level is as shown by hatching in Fig. 5. On the other hand, the sub path 12 reproduces the input image signal in 9 real gray scale levels, and the

arrangement of the light emission subfield periods for each luminance level is as shown in Fig. 6. The display characteristic of the input image signal, after processing through the sub path 12, is nonlinear; therefore, the inverse function correction for correcting the nonlinear characteristic and the error diffusion are applied to correct the nonlinear display characteristic to the linear display characteristic.

The highest luminance level that can be displayed on the PDP 4 via the sub path 12 is 8 with a 4-bit output, while the highest luminance level of the input image signal is 255 with an 8-bit input. Accordingly, the gain control circuit 122 multiplies the input image signal with a gain coefficient $8\times2^{8-4}/255 = 128/255$. As a result of the multiplication with this gain coefficient, the error diffusion circuit 123 at the next stage can apply error diffusion over the entire range of the input image signal. The gain control circuit 122 can be constructed from a conventional multiplier or from a RAM or a ROM.

By applying error diffusion to the image signal obtained via the gain control circuit 122, the error diffusion circuit 123 simulates intermediate gray levels to increase the number of gray scale levels. Since the number of reproducible gray scale levels in the sub path 12 is 9, the output bit count of the error diffusion circuit 123 is 4. The data matching circuit 124 is provided to match the luminance level in the sub path 12 to the luminance level in the main path 11.

Based on the path select/switch signal supplied from the image feature judging section 14, the switch circuit 13 switches the path to be used in accordance with the input image signal. Accordingly, for the RGB signals constituting the input image signals, the path switching is performed for each of the R, G, and B colors independently of each other. Therefore, even in the case of the RGB signals for the same pixel, there can occur cases where, for example, the R signal is processed

through the main path 11 while the G and B signals are processed through the sub path 12.

Next, the operation of the image feature judging circuit 14 will be described. The image feature judging circuit 14 detects an image on which a moving image false contour is likely to occur, and generates and outputs the path select/switch signal for instructing the switch circuit 13 to switch the path so that pixel data forming such an image will be processed through the sub path 12.

As earlier described, the moving image false contour tends to occur at specific luminance levels, that is, at such luminance levels where the light emission subfield period greatly varies along the time axis even though the gray scale level changes only slightly. In view of this, the level detection circuit 145, based on the output of the error diffusion circuit 112 in the main path 11, supplies to the second judging circuit 146 a signal for controlling the sensitivity with which to switch the path to the sub path 12 by the path select/switch signal output from the first judging circuit 144. More specifically, for a luminance level where the moving image false contour is noticeable, the level detection circuit 145 outputs to the second judging circuit 146 a signal that increases the sensitivity with which to switch to the sub path 12; on the other hand, for a luminance level where the moving image false contour is inherently not easily detectable even when the image has a portion containing much motion, the level detection circuit 145 outputs a signal that reduces the sensitivity with which to switch to the sub path 12.

The reason that the level detection circuit 145 detects the luminance level by using the output image data from the main path 11 is that the luminance level where the moving image false contour is noticeable is substantially determined by the arrangement of the light emission subfield periods in the main path 11. In a portion rich in high-frequency components within an

image, that is, in an edge portion, the difference between fields is detected even in an area where there is only a small amount of motion and, as a result, the amount of motion is detected larger than necessary. In view of this, the edge detection circuit 142 detects an edge portion within the image based on the input image signal, and supplies the result to the first judging circuit 144. Then, the first judging circuit 144 normalizes the amount of motion, that is, the degree of motion, by dividing the difference by the edge component. As a result, the amount of motion in the edge portion is reduced, and the first judging circuit 144 generates and outputs the path select/switch signal so that the edge portion will not be processed through the main path 11.

Furthermore, since the moving image false contour becomes noticeable in a portion where gray scale changes smoothly or mildly, the false contour is not easily detectable in a portion rich in high-frequency components within an image. This characteristic is also an important factor to be considered when making a decision for the path switching; therefore, based on the input image signal, the edge detection circuit 142 outputs to the first judging circuit 144 a signal for controlling the sensitivity with which the path is switched to the sub path 12 by the path select/switch signal output from the second judging circuit 146. More specifically, the sensitivity with which to switch the path to the sub path 12 is controlled so that low-frequency regions where gray scale changes smoothly can be easily processed through the sub path 12, in other words, edge portions can be easily processed through the main path 11.

The motion region detection circuit 143 detects a region containing motion within the image based on the smallest value of the difference from the image one field back and the difference from the image two fields back obtained from the luminance signal, and supplies the result of the detection to the first judging circuit 144.

Further, the edge detection circuit 142 calculates a horizontal edge (horizontal line) and a vertical edge (vertical line) from the luminance signal, and obtains the amount of edge by mixing these edges. The amount of edge thus obtained is supplied to the first judging circuit 144. Therefore, based on the output information from the motion region detection circuit 143 and the edge detection circuit 142, the first judging circuit 144 judges pixels that tend to cause a moving image false contour, and supplies the result of the judgment to the second judging circuit 145.

The level detection circuit 145 detects the luminance level based on a corresponding one of the RGB signals that has been output from the main path 11. The luminance level detected by the level detection circuit 145 is supplied to the second judging circuit 146. Therefore, based on the result of the judgment from the first judging circuit 144 and the luminance level detected by the level detection circuit 145, the second judging circuit 146 generates the path select/switch signal for causing the path to be switched so that pixel data greater than a prescribed level will be processed through the sub path 12, and supplies the thus generated signal to the switch circuit 13. The level detection circuit 145 and the second judging circuit 146 together constitute a level judging section.

In this way, the path is automatically switched so that normally the input image signal is processed through the main path 11 which ensures an adequate number of gray scale levels, and so that the input image signal is processed through the sub path 12 only for pixel data that tends to cause a moving image false contour. Therefore, normally the input image signal is processed through the main path 11 which provides an extremely good S/N ratio and ensures a sufficient number of real gray scale levels for the PDP, and the processed image is presented for display on the PDP 4; on the other hand,

for an image portion where a moving image false contour is highly likely to occur, the image signal is processed through the sub path 12 which has a very high capability to eliminate the moving image false contour though the S/N ratio somewhat drops, and the processed image is presented for display on the PDP 4. In this case, since the light emission subfield periods in the main path 11 and the light emission subfield periods in the sub path 12 have a close relationship to each other, the path switching portion (boundary) is hardly noticeable.

Figure 7 is a block diagram showing one example of the image feature judging section in the image processing circuit of Fig. 3.

As shown in Fig. 7, the edge detection circuit 142 comprises 1H delay circuits 1421 and 1422, a delay circuit 1423, subtraction circuits 1424 and 1425, absolute value circuits 1426 and 1427, maximum value detection circuits 1428 and 1429, multiplication circuits 1470, 1471, and 1473, and an addition circuit 1472. The motion region detection circuit 143 comprises 1V delay circuits 1431 and 1432, subtraction circuits 1433 and 1434, absolute value circuits 1435 and 1436, and a minimum value detection circuit 1437. Here, 1H indicates one horizontal scan period of the input image signal, and 1V indicates one vertical scan period of the input image signal.

The first judging circuit 144 comprises a division circuit 1441, on the output side of which are connected an isolated point eliminating circuit 1442, a temporal filter 1443, and a two-dimensional low-pass filter (LPF) 1444. The level detection circuit 145 comprises a sensitivity RAM 1451, a multiplication circuit 1452, and a comparator 1453.

In the edge detection circuit 142, the subtraction circuit 1424 obtains the difference between the current input luminance signal Y and the input luminance signal Y two H's back, and the absolute value circuit 1426 obtains

the absolute value of the difference fed from the subtraction circuit 1424. Of the absolute values obtained by the absolute value circuit 1426, the maximum value detection circuit 1428 detects, for example, the three largest absolute values and outputs them to the multiplication circuit 1470. The multiplication circuit 1470 is supplied with a coefficient that determines the sensitivity with which to detect a horizontal edge extending in a horizontal direction, and the output of the multiplication circuit 1470 is supplied to the addition circuit 1472.

The delay circuit 1423 delays the input luminance signal Y on a pixel-by-pixel basis (D), and the subtraction circuit 1425 obtains the difference between pixels of the input image signal. The absolute value circuit 1427 obtains the absolute value of the difference fed from the subtraction circuit 1425 and, of the absolute values obtained by the absolute value circuit 1427, the maximum value detection circuit 1429 detects, for example, the three largest absolute values and outputs them to the multiplication circuit 1471. The multiplication circuit 1471 is supplied with a coefficient that determines the sensitivity with which to detect a vertical edge extending in a vertical direction, and the output of the multiplication circuit 1471 is supplied to the addition circuit 1472. The output of the addition circuit 1472 is supplied to the multiplication circuit 1473 where it is multiplied with a coefficient that determines the edge sensitivity as a whole. The multiplication circuit 1473 thus outputs a signal indicating the amount of edge, which is supplied to the division circuit 1441.

In the motion region detection circuit 143, the subtraction circuit 1433 obtains the difference of the input luminance signal Y between two adjacent field periods and supplies it to the absolute value circuit 1435, while the subtraction circuit 1434 obtains the

difference of the input luminance signal Y between two adjacent frame periods and supplies it to the absolute value circuit 1436. Therefore, the absolute value circuit 1435 obtains the absolute value of the difference between the input luminance signal Y in the current field period and the input luminance signal Y one field period back, and supplies it to the minimum value detection circuit 1437.

The absolute value circuit 1436 obtains the absolute value of the difference between the input luminance signal Y in the current field period and the input luminance signal Y two field periods back, and supplies it to the minimum value detection circuit 1437 which, of the absolute values supplied from the absolute value circuits 1435 and 1436, supplies the smallest value to the division circuit 1441 as a signal indicating the amount of motion. When non-interlaced scanning is employed, a difference may be detected between an odd-numbered field period and the even-numbered field period that follows, even when actually there is no motion in the image. Therefore, the difference is obtained between the input luminance signal Y in the current field period and the input luminance signal Y two field periods back as well as the difference between the input luminance signal Y in the current field period and the input luminance signal Y one field period back, and the amount of motion is obtained from the smallest value of their absolute values.

The absolute value of the difference obtained from each of the absolute value circuits 1435 and 1436 is, for example, in units of levels/field, and the amount of motion obtained from the minimum value detection circuit 1437 is, for example, in units of dots/field. Here, the amount of motion is expressed as Amount of Motion (dots/field) = {(|difference (minimum value) (levels/field)|)} ÷ {|slope (levels/dot)|}.

The division circuit 1441 normalizes the degree of

motion in the image, i.e., the amount of motion, by dividing the amount of motion obtained from the minimum value detection circuit 1437 by the amount of edge obtained from the multiplication circuit 1473. The amount of motion normalized by the division circuit 1441 is supplied to the multiplication circuit 1452 in the level detection circuit 145 via the isolated point eliminating circuit 1442, the temporal filter 1443, and the two-dimensional LPF 1444.

The isolated point eliminating circuit 1442 is provided to eliminate isolated image data such as noise. For example, if, in a given region within the image, only one pixel is in motion while its surrounding pixels do not exhibit any motion, that one pixel can be regarded as noise, and in such cases, the isolated point is eliminated by the isolated point eliminating circuit 1442. More specifically, the amount of motion of each pixel in each line is compared with a threshold value, and any pixel whose amount of motion is smaller than the threshold value can be eliminated as an isolated point by regarding it as a non-moving pixel.

The temporal filter 1443 is provided to correct the falling of the level of motion-exhibiting pixel data so that the level falls mildly along the time axis. For example, when a particular pixel within the image, which is in motion, stops abruptly, its motion does not appear stopping immediately to the human eye because of the persistence of human vision, etc. even though that particular pixel has stopped when seen in terms of the image data. Therefore, the temporal filter 1443 corrects the falling of the level of the motion-exhibiting pixel data so that the level falls mildly along the time axis, thereby making the image displayed on the PDP 4 match the characteristics of human vision, thus reducing the unnaturalness of the image. In a specific method, the temporal filter 1443 obtains the maximum value from the amount of motion obtained from the isolated point

eliminating circuit 1442 and the value read out of the memory described later, multiplies the maximum value with a coefficient smaller than 1, and stores the result in the memory. The obtained maximum value is output from the temporal filter 1443 and fed to the two-dimensional LPF 1444. That is, since the amount of motion stored in the memory decreases little by little, the amount of motion being output from the temporal filter 1443 decreases mildly even when the actual amount of motion has dropped to zero.

The two-dimensional LPF 1444 corrects data of one pixel based on the data of its surrounding pixels, and thereby averages the pixel data within a certain range to prevent only one pixel from showing a level extremely different from the levels of its surrounding pixels. That is, the two-dimensional LPF 1444 corrects the amount of motion in two-dimensional space. The two-dimensional LPF 1444 having such a function is well known in the art.

The level detection circuit 145 comprises three detection circuit sections one for each of the RGB signals, each section comprising the sensitivity RAM 1451, multiplication circuit 1452, and comparator 1453. For example, the output of the main path 11 for the R signal is supplied to the sensitivity RAM 1451 in the detection circuit section for the R signal, and the amount of motion supplied from the two-dimensional LPF 1444 is multiplied in the multiplication circuit 1452 by the coefficient read out of the sensitivity RAM 1451. The amount of motion thus multiplied is supplied to the comparator 1453. The comparator 1453 compares the amount of motion supplied from the multiplication circuit 1452 with a threshold value; if the amount of motion supplied from the multiplication circuit 1452 is larger than the threshold value, the comparator 1453 outputs a path select/switch signal for switching the R signal path to the sub path 12. In like manner, the detection circuit sections for the G and B signals each output a path

select/switch signal for switching the G or B signal path based on the output of the main path 11 for the G or B signal, respectively.

Therefore, in each of the RGB processing systems, normally the input image signal (corresponding one of the RGB signals) is processed through the main path that ensures a relatively large number of gray scale levels, but pixel data that tends to cause a moving image false contour is processed through the sub path 12 by automatically switching the path to the sub path 12. In principle, the S/N ratio of the image displayed based on the image data processed through the sub path 12 is somewhat inferior to that of the image displayed based on the image data processed through the main path 11, but since the image displayed based on the image data processed through the sub path 12 represents a moving image portion, the degradation of the S/N ratio is hardly noticeable to the human eye and, therefore, does present any problem in practice. In this case, the calculation parameters used in the main path 11 and the sub path 12 are set so that the degradation of the S/N ratio caused by processing the data through the sub path 12 will not become noticeable to the human eye. Here, as a matter of course, the calculation parameters used in the main path 11 and the sub path 12 need to be re-set to optimum parameters each time the driving sequence for the PDP 4 or the subfield structure for the PDP 4 is changed.

In the prior art, there is also proposed, in JPP'649, a display apparatus and a display driving method in which, by using an error diffusion technique, the maximum gray scale level and the number of reproducible gray scale levels are made sufficiently large without increasing the number of subfields, while at the same time achieving enhancement in the reproducibility of low gray scale levels.

In the prior art, various display driving techniques for reducing the moving image false contour have been

proposed as described above. Specifically, the image processing circuit in the prior art plasma display apparatus shown in Fig. 3 (for example, JPP'455), for example, provides an excellent technique in that it can completely suppress the occurrence of a moving image false contour, but there has been the problem that the image region processed through the sub path contains noise due to error diffusion, that is, the image region appears like noise due to the reduced number of gray scale levels. In particular, when the number of gray scale levels in the main path is made large, the number of gray scale levels where a moving image false contour tends to occur increases, resulting in an increase in the number of image regions to be switched to the moving path, and hence an increase in noise, causing a degradation of picture quality.

The prior art also proposes a technique for reducing the degradation of picture quality caused when the number of gray scale levels in the main path is made large (for example, JPP'101), but it has technically been difficult to detect a color space that cannot be recognized by human vision.

There is also proposed in the prior art a display apparatus and a display driving method in which the number of gray scales is increased by error diffusion (for example, JPP'649), but this increases the amount and cost of hardware since the gray scale conversion table requires the provision of a memory.

An object of the present invention to provide a display apparatus and a display driving method that can effectively eliminate the occurrence of a moving image false contour without incurring a substantial increase in cost.

According to the present invention, the weight of each subfield is set small in the subfield arrangement in the main path so that a moving image false contour does not easily occur, and provisions are made to prevent a

situation where, of the subfields to be set for light emission when displaying gray scale, the most heavily weighted subfield alone is set for light emission.

In this case, the total number of gray scale levels decreases since the weight of each field is set small, but according to the present invention, a first subfield arrangement setting unit, a second subfield arrangement setting unit, and a sub gain control circuit work together to increase the apparent number of gray scale levels. More specifically, gray scale levels that cannot be reproduced by combining the plurality of subfields are simulated by applying error diffusion between the gray scale levels that can be reproduced by combining the plurality of subfields. Furthermore, since the number of gray scale levels is increased by performing computations in the sub gain control circuit, the present invention eliminates the need for a gray scale conversion table and the memory capacity can be reduced.

As a result, moving image false contours do not easily occur at most of the gray scale levels generated in the main path, and the path is switched to the sub path only for the remaining gray scale levels where a moving image false contour is likely to occur. This serves to greatly reduce the noise that occurs due to error diffusion in the sub path.

Below, embodiments of a display apparatus and a display driving method according to the present invention will be described in detail with reference to the drawings.

Figure 8 is a block diagram showing one example of an image processing circuit in the plasma display apparatus according to the present invention, which is applied, for example, as the image processing circuit 1 in the plasma display apparatus previously shown in Fig. 1. In Fig. 8, reference numeral 1 is the image processing circuit, 11 is a main path, 12 is a sub path, 13 is a switch circuit, and 14 is an image feature

judging section. Further, reference numeral 111 is a gain control circuit, 112 is an error diffusion circuit, 113 is a sub gain control circuit, 121 is a distortion correction circuit, 122 is a gain control circuit, 123 is an error diffusion circuit, and 124 is a data matching circuit. On the other hand, reference numeral 141 is an RGB matrix circuit, 142 is an edge detection circuit, 143 is a motion region detection circuit, 144 is a first judging circuit, 145 is a level detection circuit, and 146 is a second judging circuit.

As is apparent from a comparison between Fig. 8 and the previously shown Fig. 3, the image processing circuit in the plasma display apparatus according to the present invention shown in Fig. 8 differs from the prior art image processing circuit 1 shown in Fig. 3 by the inclusion of the sub gain control circuit 113 which is inserted between the gain control circuit 111 and the error diffusion circuit 112 in the main path 11. The effect, etc. of providing the sub gain control circuit 113 in addition to the gain control circuit 111 in the present invention will be described in detail later with reference to Figs. 50 to 60.

As shown in Figs. 8 and 50A, in the main path 11, an input image signal, for example, with 256 gray scale levels, is supplied to the gain control circuit 111 where it is multiplied by 219/255, and a signal (first intermediate image signal) AA with 220 gray scale levels is output from the gain control circuit 111. The first intermediate image signal AA with 220 gray scale levels is supplied to the sub gain control circuit 113 where it is multiplied by 147/219, and a signal (second intermediate image signal) BB with 148 gray scale levels is output from the sub gain control circuit 113. Further, the second intermediate image signal BB with 148 gray scale levels is supplied to the error diffusion circuit 112, and a signal (first image signal: output signal of the main path 11) CC with 148 gray scale levels

is output from the error diffusion circuit 112. In the image processing circuit of the plasma display apparatus shown in Fig. 8, the sub path 12, the switch circuit 13, and the image feature judging section 14 are essentially the same in configuration as those previously shown in Fig. 3, and the description thereof will not be repeated here. Further, in the image processing circuit of the plasma display apparatus shown in Fig. 8, the image feature judging section 14 is the same as the image feature judging section described with reference to Figs. 3 and 7, and the description thereof will also be omitted here.

Figures 9 to 12 are diagrams showing one example of a subfield light emission table which is applied to the plasma display apparatus according to the present invention and used when producing a gray scale display in the main path. Figure 13 is a diagram showing one example of a subfield light emission table for the sub path, which is applied to the plasma display apparatus according to the present invention, and which corresponds to the subfield light emission table for the main path shown in Figs. 9 to 12.

In the subfield light emission table shown in Figs. 9 to 12, the weights between the subfields (SFs) are set small and, in addition, of the subfields to be set for light emission when displaying an arbitrary gray scale level except low gray scale levels, the most heavily weighted subfield is prohibited from being set for light emission independently of the others.

More specifically, as shown in Figs. 9 to 12, the weights of SF1 to SF10 are set in the ratio of SF1:SF2:SF3:SF4:SF5:SF6:SF7:SF8:SF9:SF10 = 1:2:4:8:12:16:20:24:28:32, that is, the weights between the SFs are set small. In addition, except at low gray scale levels (gray scale levels: 1, 2, 4, 8), the most heavily weighted subfield will not be set for light emission independently of the others in the case of gray

scale levels (gray scale levels: 16, 28, 44, 64, 88, 116) where the next SF is set for light emission.

As a result, moving image false contours do not easily occur at most gray scale levels, but at some gray scale levels, the moving image false contour does occur. Therefore, for such gray scale levels, the path is switched from the main path to the sub path to completely eliminate the occurrence of the moving image false contour.

That is, as shown in Fig. 13, for gray scale levels where the moving image false contour is likely to occur (for example, gray scale levels: 2, 4, 8, 16, 28, 44, 64, 88, 116, 148), the path is switched from the main path 11 to the sub path 12 to completely eliminate the occurrence of the moving image false contour. The subfield light emission table shown in Figs. 9 to 12 is applied to the main path 11 in the image processing circuit shown in Fig. 8, and can also be used by switching to the sub path 12 for the above-listed specific grayscale levels, but even when this subfield light emission table is applied to an image processing circuit that does not have a sub path, and all the gray scale levels are displayed in accordance with the combinations shown in the subfield light emission table of Figs. 9 to 12, the moving image false contour can be greatly reduced compared with the prior art driving method (for example, SF1:SF2:SF3:SF4:SF5:SF6 = 1:2:4:8:16:32).

Figures 14 to 17 are diagrams showing another example of the subfield light emission table which is applied to the plasma display apparatus according to the present invention and used when producing a gray scale display in the main path. Figure 18 is a diagram showing one example of the subfield light emission table for the sub path, which is applied to the plasma display apparatus according to the present invention, and which corresponds to the subfield light emission table for the main path shown in Figs. 14 to 17. As is apparent from a

comparison between Figs. 14 to 17 and Figs. 9 to 12, in the subfield light emission table shown in Figs. 14 to 17 the weights are assigned to SF1 to SF10 in the reverse order from those assigned in the subfield light emission table shown in Figs. 9 to 12 (that is, SF1:SF2:SF3:SF4:SF5:SF6:SF7:SF8:SF9:SF10 = 32:28:24:20:16:12:8:4:2:1).

In the subfield light emission table shown in Figs. 14 to 17 also, the weights between the subfields (SFs) are set small and, in addition, of the subfields to be set for light emission when displaying an arbitrary gray scale level except low gray scale levels (gray scale levels: 1, 2, 4, 8), the most heavily weighted subfield is prohibited from being set for light emission independently of the others. As a result, moving image false contours do not easily occur at most gray scale levels, but at some gray scale levels, the moving image false contour does occur. Therefore, by switching the path from the main path to the sub path for such gray scale levels (for example, gray scale levels: 2, 4, 8, 16, 28, 44, 64, 88, 116, 148), the occurrence of the moving image false contour can be completely eliminated.

Figure 19 is a block diagram schematically showing a sub gain control circuit in a first embodiment of the plasma display apparatus according to the present invention, and Fig. 20 is a diagram for explaining the sub gain control circuit shown in Fig. 19. The following description assumes the use of the main path subfield light emission table shown in Figs. 9 to 12 and the sub path subfield light emission table shown in Fig. 13.

The sub gain control circuit shown in Fig. 19 performs computations that satisfy the relations shown in Fig. 20, and comprises a computation circuit 311, multiplication circuits 312 to 314, addition circuits 315 to 317, a selection circuit 318, and a remainder calculation circuit 319. The computation circuit 311 receives the input signal AA (the first intermediate

image signal with 220 gray scale levels output from the gain control circuit 111), divides it by a coefficient C=3, and outputs the integer part. The result of the computation [AA/3] is supplied to the multiplication circuits 312 and 313.

The output signal of the computation circuit 311 is multiplied by "-1" in the multiplication circuit 312, and the output signal of the multiplication circuit 312 is summed with the input signal AA in the addition circuit 315. As a result, BB = AA-[AA/3] is obtained from the path P11. On the other hand, the output signal of the computation circuit 311 supplied to the multiplication circuit 313 is multiplied by "+1", the output signal of the multiplication circuit 313 is summed with "+1" in the addition circuit 316, the output signal of the addition circuit 316 is summed with the input signal AA in the addition circuit 317, and the sum is multiplied by "1/2" in the multiplication circuit 314. As a result, BB = (AA+[AA/3]+1)/2 is obtained from the path P12.

The selection circuit 318 selects the output signal of the path P11 or the output signal of the path P12 in accordance with the output of the remainder calculation circuit 319; that is, when the remainder of AA/3 is zero (exactly divisible), the path P11 (the output signal of the addition circuit 315) is selected, while when the remainder of AA/3 is not zero (1 or 2, that is, not exactly divisible), the path P12 (the output signal of the multiplication circuit 314) is selected, and the thus selected signal is output as the second intermediate image signal BB.

In this way, the sub gain control circuit according to the first embodiment shown in Fig. 19 performs computations that satisfy the relations shown in Fig. 20; as shown in Fig. 20, in the first embodiment, the entire gray scale range is divided into two regions, region R11 and region R12, so that the ratio between the input signal AA and the output signal BB becomes approximately

equal to 2/3.

In the region R11, the relation $3\times K \leq$ input signal AA $< 3\times K+1$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as BB = AA - [AA/3]. On the other hand, in the region R12, the relation $3\times K+1 \leq$ input signal AA $< 3\times(K+1)$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as BB = (AA+[AA/3]+1)/2.

Table 1 below shows the relationship between the subfields SF1 to SF10 and the weights, which is stored in the SF weight table 33 (see Fig. 1) according to the first embodiment; as shown, the weights are multiplied by 1.5 (3/2). That is, the gray scale (number of gray scale levels: 148) resulting from the multiplication by 2/3 in the sub gain control circuit of the first embodiment is converted back to the original gray scale (number of gray scale levels: 220) for display on the PDP 4.

[TABLE 1]

	SF1	SF2	SF3	SF4	SF5	SF6	SF7	SF8	SF9	SF10
WEIGHT	1	3	6	12	18	24	30	36	42	48

Figures 21 to 26 are diagrams for explaining the operation of the sub gain control circuit shown in Fig. 19, and illustrate how the input signal AA with 220 gray scale levels input to the sub gain control circuit 113 is output as the output signal BB with 147 gray scale levels by selecting the path P11 or the path 12 in accordance with the output of the remainder calculation circuit 319, and how the output signal BB is converted back to the image signal with 220 gray scale levels in accordance with the SF weight table 33.

Figure 27 is a block diagram schematically showing a sub gain control circuit in a second embodiment of the plasma display apparatus according to the present invention, and Fig. 28 is a diagram for explaining the sub gain control circuit shown in Fig. 27.

The sub gain control circuit shown in Fig. 27 performs computations that satisfy the relations shown in Fig. 28, and comprises a computation circuit 321, multiplication circuits 322 to 325, addition circuits 326 to 330, a selection circuit 331, and a remainder calculation circuit 332. The computation circuit 321 receives the input signal AA (the first intermediate image signal with 184 gray scale levels output from the gain control circuit 111), divides it by a coefficient C=5, and outputs the integer part. The result of the computation [AA/5] is supplied to the multiplication circuits 322, 323, and 324.

The output signal of the computation circuit 321 is multiplied by "-1" in the multiplication circuit 322, the resulting product is summed with "-1" in the addition circuit 326, and the output signal of the addition circuit 326 is summed with the input signal AA in the addition circuit 327. As a result, BB = AA-[AA/5]-1 is obtained from the path P23. On the other hand, the output signal of the computation circuit 321 supplied to the multiplication circuit 323 is multiplied by "-1", and the output signal of the multiplication circuit 323 is summed with the input signal AA in the addition circuit 328. As a result, BB = AA- [AA/5] is obtained from the path P21. Further, the output signal of the computation circuit 321 supplied to the multiplication circuit 324 is multiplied by "+3", the output signal of the multiplication circuit 324 is summed with "+1" in the addition circuit 329, the output signal of the addition circuit 329 is summed with the input signal AA in the addition circuit 330, and the sum is multiplied by "1/2" in the multiplication circuit 325. As a result, BB = (AA+[AA/5]×3+1)/2 is obtained from the path P22.

The selection circuit 331 selects the output signal of one of the paths P21 to P23 in accordance with the output of the remainder calculation circuit 332; that is, when the remainder of AA/5 is zero, the path P21 (the

output signal of the addition circuit 328) is selected, and when the remainder of AA/5 is 1 or 2, the path P22 (the output signal of the multiplication circuit 325) is selected, while when the remainder of AA/5 is 3 or 4, the path P23 (the output signal of the addition circuit 327) is selected, and the thus selected signal is output as the second intermediate image signal BB.

In this way, the sub gain control circuit according to the second embodiment shown in Fig. 27 performs computations that satisfy the relations shown in Fig. 28; as shown in Fig. 28, in the second embodiment, the entire gray scale range is divided into three regions, region R21, region R22, and region R23, so that the ratio between the input signal AA and the output signal BB becomes approximately equal to 4/5.

In the region R21, the relation $5\times K \leq$ input signal AA $< 5\times K+1$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as BB = AA-[AA/5]. On the other hand, in the region R22, the relation $5\times K+1 \leq$ input signal AA $< 5\times K+3$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as BB = (AA+[AA/5]×3+1)/2. Further, in the region R23, the relation $5\times K+3 \leq$ input signal AA $< 5\times(K+1)$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as BB = AA-[AA/5]-1.

Table 2 below shows the relationship between the subfields SF1 to SF10 and the weights, which is stored in the SF weight table 33 according to the second embodiment; as shown, the weights are multiplied by 1.25 (5/4). That is, the gray scale (number of gray scale levels: 148) resulting from the multiplication by 4/5 in the sub gain control circuit of the second embodiment is converted back to the original gray scale (number of gray scale levels: 184) for display on the PDP 4.

[TABLE 2]

	SF1	SF2	SF3	SF4	SF5	SF6	SF7	SF8	SF9	SF10
WEIGHT	1	3	5	10	15	20	25	30	35	40

Figures 29 to 33 are diagrams for explaining the operation of the sub gain control circuit shown in Fig. 27, and illustrate how the input signal AA with 184 gray scale levels input to the sub gain control circuit 113 is output as the output signal BB with 148 gray scale levels by selecting one of the paths P21 to P23 in accordance with the output of the remainder calculation circuit 332, and how the output signal BB is converted back to the image signal with 184 gray scale levels in accordance with the SF weight table 33.

Figure 34 is a block diagram schematically showing a sub gain control circuit in a third embodiment of the plasma display apparatus according to the present invention, and Fig. 35 is a diagram for explaining the sub gain control circuit shown in Fig. 34.

The sub gain control circuit shown in Fig. 34 performs computations that satisfy the relations shown in Fig. 35, and comprises a computation circuit 341, multiplication circuits 342 to 347, addition circuits 348 to 354, a selection circuit 355, and a remainder calculation circuit 356. The computation circuit 341 receives the input signal AA (the first intermediate image signal with 256 gray scale levels output from the gain control circuit 111), divides it by a coefficient C=7, and outputs the integer part. The result of the computation [AA/7] is supplied to the multiplication circuits 342, 343, 344, and 345.

The output signal of the computation circuit 341 is multiplied by "+5" in the multiplication circuit 342, the resulting product is summed with "+5" in the addition circuit 348, the output signal of the addition circuit 348 is summed with the input signal AA in the addition circuit 349, and the sum is multiplied by "1/3" in the

multiplication circuit 346. As a result, BB = (AA+[AA/7]×5+5)/3 is obtained from the path P34. On the other hand, the output signal of the computation circuit 341 supplied to the multiplication circuit 343 is multiplied by "-3", the resulting product is summed with "-1" in the addition circuit 350, and the output signal of the addition circuit 350 is summed with the input signal AA in the addition circuit 351. As a result, BB = AA-[AA/7]×3-1 is obtained from the path P33.

Further, the output signal of the computation circuit 341 supplied to the multiplication circuit 344 is multiplied by "-3", and the output signal of the multiplication circuit 344 is summed with the input signal AA in the addition circuit 352. As a result, BB = AA-[AA/7]×3 is obtained from the path P31. On the other hand, the output signal of the computation circuit 341 supplied to the multiplication circuit 345 is multiplied by "+1", the resulting product is summed with "+1" in the addition circuit 353, the output signal of the addition circuit 353 is summed with the input signal AA in the addition circuit 354, and the sum is multiplied by "1/2" in the multiplication circuit 347. As a result, BB = (AA+[AA/7]+1)/2 is obtained from the path P32.

The selection circuit 355 selects the output signal of one of the paths P31 to P34 in accordance with the output of the remainder calculation circuit 356; that is, when the remainder of AA/7 is zero, the path P31 (the output signal of the addition circuit 352) is selected, and when the remainder of AA/7 is 1 or 2, the path P32 (the output signal of the multiplication circuit 347) is selected, while when the remainder of AA/7 is 3, the path P33 (the output signal of the addition circuit 351) is selected, and when the remainder of AA/7 is 4, 5, or 6, the path P34 (the output signal of the multiplication circuit 346) is selected, and the thus selected signal is output as the second intermediate image signal BB.

In this way, the sub gain control circuit according to the third embodiment shown in Fig. 34 performs computations that satisfy the relations shown in Fig. 35; as shown in Fig. 35, in the third embodiment, the entire gray scale range is divided into four regions, region R31, region R32, region R33, and region R34, so that the ratio between the input signal AA and the output signal BB becomes approximately equal to 4/7.

In the region R31, the relation $7\times K \leq$ input signal AA $< 7\times K+1$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as $BB = AA-[AA/7]\times 3$. On the other hand, in the region R32, the relation $7\times K+1 \leq$ input signal AA $< 7\times K+3$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as $BB = (AA+[AA/7]+1)/2$. Further, in the region R33, the relation $7\times K+3 \leq$ input signal AA $< 7\times K+4$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as $BB = AA-[AA/7]\times 3-1$. In the region R34, the relation $7\times K+4 \leq$ input signal AA $< 7\times(K+1)$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as $BB = (AA+[AA/7]\times 5+5)/3$.

Table 3 below shows the relationship between the subfields SF1 to SF10 and the weights, which is stored in the SF weight table 33 according to the third embodiment; as shown, the weights are multiplied by 1.75 (7/4). That is, the gray scale (number of gray scale levels: 148) resulting from the multiplication by 4/7 in the sub gain control circuit of the third embodiment is converted back to the original gray scale (number of gray scale levels: 256) for display on the PDP 4. Here, as shown in Tables 1 to 3, the weight of the first subfield SF1 is 1, while the weight of the second subfield SF2 is 3 (or not smaller than 3).

[TABLE 3]

	SF1	SF2	SF3	SF4	SF5	SF6	SF7	SF8	SF9	SF10
WEIGHT	1	3	7	14	21	28	35	42	49	56

Figures 36 to 42 are diagrams for explaining the operation of the sub gain control circuit shown in Fig. 34, and illustrate how the input signal AA with 256 gray scale levels input to the sub gain control circuit 113 is output as the output signal BB with 148 gray scale levels by selecting one of the paths P31 to P34 in accordance with the output of the remainder calculation circuit 356, and how the output signal BB is converted back to the image signal with 256 gray scale levels in accordance with the SF weight table 33.

Figure 43 is a block diagram schematically showing a sub gain control circuit in a fourth embodiment of the plasma display apparatus according to the present invention, and Fig. 44 is a diagram for explaining the sub gain control circuit shown in Fig. 43.

The sub gain control circuit shown in Fig. 43 performs computations that satisfy the relations shown in Fig. 44, and comprises a computation circuit 361, multiplication circuits 362 to 365, addition circuits 366 to 368, a selection circuit 369, and a remainder calculation circuit 370. The computation circuit 361 receives the input signal AA (the first intermediate image signal with 184 gray scale levels output from the gain control circuit 111), divides it by a coefficient C=5, and outputs the integer part. The result of the computation [AA/5] is supplied to the multiplication circuits 362 and 363.

The output signal of the computation circuit 361 is multiplied by "-1" in the multiplication circuit 362, and the output signal of the multiplication circuit 362 is summed with the input signal AA in the addition circuit 366. As a result, BB = AA-[AA/5] is obtained from the path P41. On the other hand, the output signal of the

computation circuit 361 supplied to the multiplication circuit 363 is multiplied by "+1", the resulting product is summed with "+1" in the addition circuit 367, the output signal of the addition circuit 367 is summed with the input signal AA in the addition circuit 368, and the sum is multiplied by "1/4" in the multiplication circuit 365. As a result, BB = (AA×3+[AA/5]+1)/4 is obtained from the path P42.

The selection circuit 369 selects the output signal of the path P41 or the output signal of the path P42 in accordance with the output of the remainder calculation circuit 370; that is, when the remainder of AA/5 is zero, the path P41 (the output signal of the addition circuit 366) is selected, while when the remainder of AA/5 is 1, 2, 3, or 4, the path P42 (the output signal of the multiplication circuit 365) is selected, and the thus selected signal is output as the second intermediate image signal BB.

In this way, the sub gain control circuit according to the fourth embodiment shown in Fig. 43 performs computations that satisfy the relations shown in Fig. 44; as shown in Fig. 44, in the fourth embodiment, the entire gray scale range is divided into two regions, region R41 and region R42, so that the ratio between the input signal AA and the output signal BB becomes approximately equal to 4/5.

In the region R41, the relation $5\times K \leq$ input signal AA $< 5\times K+1$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as BB = AA-[AA/5]. On the other hand, in the region R42, the relation $5\times K+1 \leq$ input signal AA $< 5\times(K+1)$ holds, and the mathematical equation between the input signal AA and the output signal BB is given as BB = (AA×3+[AA/5]+1)/4.

In the fourth embodiment, the output signal BB to be generated in the region R42 is generated from a smaller

number of gray scale levels than the number of gray scale levels of the input signal AA. More specifically, gray scale levels 2, 3, and 4, for example, are achieved by the diffusion of the weight 1 and the weight 5. In the fourth embodiment, the circuit is simplified by reducing the number of divided regions compared with the previously described second embodiment. That is, in the fourth embodiment, since the sub gain control circuit can be constructed using a similar configuration to the sub gain control circuit of the previously described first embodiment, the sub gain control circuit of the first embodiment and the sub gain control circuit of the fourth embodiment can be implemented using the same circuit but by changing the parameter. Further, since the parameter is approximated by the coefficient (n-1)/(m-1), the linearity of the display gray scale can be improved.

The relationship between the subfields SF1 to SF10 and the weights, stored in the SF weight table 33 according to the fourth embodiment, is the same as that previously shown in Table 2, and therefore, the weights are multiplied by 1.25 (5/4). That is, the gray scale (number of gray scale levels: 148) resulting from the multiplication by 4/5 in the sub gain control circuit of the fourth embodiment is multiplied by 5/4 and thus converted back to the original gray scale (number of gray scale levels: 184) for display on the PDP 4.

Figures 45 to 49 are diagrams for explaining the operation of the sub gain control circuit shown in Fig. 43, and illustrate how the input signal AA with 184 gray scale levels input to the sub gain control circuit 113 is output as the output signal BB with 148 gray scale levels by selecting the path P41 or the path 42 in accordance with the output of the remainder calculation circuit 370, and how the output signal BB is converted back to the image signal with 184 gray scale levels in accordance with the SF weight table 33.

Figure 50 is a block diagram of essential portions,

showing a comparison between the configuration in which the sub gain control circuit is used and the configuration in which the sub gain control circuit is not used in the plasma display apparatus: Fig. 50A shows the case in which the sub gain control circuit is used, and Fig. 50B shows the case in which the sub gain control circuit is not used.

First, when the sub gain control circuit 113 is used, as shown in Fig. 50A, the input image signal, for example, with 256 gray scale levels, is multiplied by 219/255 in the gain control circuit 111 and thus converted (compressed) to the first intermediate image signal A1 (the first intermediate image signal AA) with 220 gray scale levels, which is supplied to the sub gain control circuit 113. In the sub gain control circuit 113, as previously described with reference to Figs. 19 to 26, the first intermediate image signal A1 with 220 gray scale levels is multiplied by 2/3 (147/219) and thus converted to the second intermediate image signal B1 (the second intermediate image signal BB) with 148 gray scale levels, which is supplied to the error diffusion circuit 112. Here, the fractional part resulting when the input image signal with 256 gray scale levels is multiplied by 219/255 in the gain control circuit 111 is passed through the sub gain control circuit 113 to the error diffusion circuit 112 where error diffusion is applied to it. Further, the fractional part of the second intermediate image signal B1 resulting when the first intermediate image signal A1 with 220 gray scale levels is multiplied by 2/3 in the sub gain control circuit 113 (the processing similar to that described with reference to Figs. 19 to 26) is also passed to the error diffusion circuit 112 where error diffusion is applied to it.

Then, the output signal of the error diffusion circuit 112 (with 148 real gray scale levels) is converted (expanded) to an image signal C1 with 220 gray scale levels by multiplying the number of gray scale

levels by 1.5 (3/2) in the SUS weight setting section (for example, the conversion table stored in the SF weight table 33 in Fig. 1, the number-of-SUSs setting circuit 34, and the controller 35). Here, the image signal C1 with 220 gray scale levels resulting from the multiplication by 3/2 in the SF weight setting section contains data obtained by error diffusion in the error diffusion circuit 112, and the PDP 4 thus simulates a 256-gray-scale display.

On the other hand, when the sub gain control circuit is not used, as shown in Fig. 50B, the input image signal, for example, with 256 gray scale levels, is multiplied by 147/255 in the gain control circuit 111 and thus converted to the intermediate image signal A2 with 148 gray scale levels, which is supplied to the error diffusion circuit 112. Here, the fractional part resulting when the input image signal with 256 gray scale levels is multiplied by 147/255 in the gain control circuit 111 is passed to the error diffusion circuit 112 where error diffusion is applied to it.

Then, the output signal of the error diffusion circuit 112 (with 148 real gray scale levels) is converted to an image signal C2 with 220 gray scale levels by multiplying it by 3/2 in the SF weight setting section (33). Here, the image signal C2 with 220 gray scale levels resulting from the multiplication by 3/2 in the SF weight setting section contains data obtained by error diffusion in the error diffusion circuit 112, and the PDP 4 thus simulates a 256-gray-scale display.

Figures 51 to 60 are diagrams for explaining the effect of using the sub gain control circuit 113 in the plasma display apparatus according to the present invention. In Figs. 51 to 60, COMPUTATION (1) in the column of "WITH SUB GAIN CONTROL CIRCUIT" corresponds to the computation in the path P11 in Fig. 19, that is, B1 = A1-[A1/3], while COMPUTATION (2) corresponds to the computation in the path P12 in Fig. 19, that is, B1 =

(A1+[A1/3]+1)/2, and the output of the path P11 or the path P12 is selected depending on whether the signal A1 is exactly divisible by 3 or not. In the case of not using the sub gain circuit, the difference between the first intermediate image signal A1 and the output image signal C2 is taken as the error of the output signal accuracy to consider the error with respect to the 220-gray-scale signal.

As can be seen from Figs. 51 to 60, when the parameter of the gain control circuit 111 is changed so that the input image signal with 256 gray scale levels is multiplied by 147/255 in the gain control circuit 111, and the resulting intermediate image signal A1 with 148 gray scale levels is supplied to the error diffusion circuit 112 whose output signal is supplied to the SF weight setting section (33) as shown in Fig. 50B, information loss (signal loss) occurs due to the signal compression performed in the gain control circuit 111.

That is, when the sub gain control circuit is used as shown in Fig. 50A, the error of the output signal accuracy (A1-C1) is zero at every gray scale level, which means that no error occurs between the input signal (the first intermediate image signal A1) and the output image signal C1 (the input signal is completely reproduced), but in the case of Fig. 50B that does not use the sub gain control circuit, an error occurs in the output signal accuracy (A1-C2) at each gray scale level, the error accumulating as much as to 70.42 gray scale levels.

In this way, the display apparatus according to the present invention is essentially different from the prior art in which the parameter of the gain control circuit is simply changed. It will also be noted that the present invention is not limited in application to plasma display apparatuses, but is also applicable to any other display apparatus that expresses luminance by varying light emission time length and achieves gray scale display by using a subfield method.

As described above, according to the present invention, a display apparatus and a display driving method that can effectively eliminate the occurrence of a moving image false contour can be provided without incurring a substantial increase in cost.

Many different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not limited to the specific embodiments described in this specification, except as defined in the appended claims.